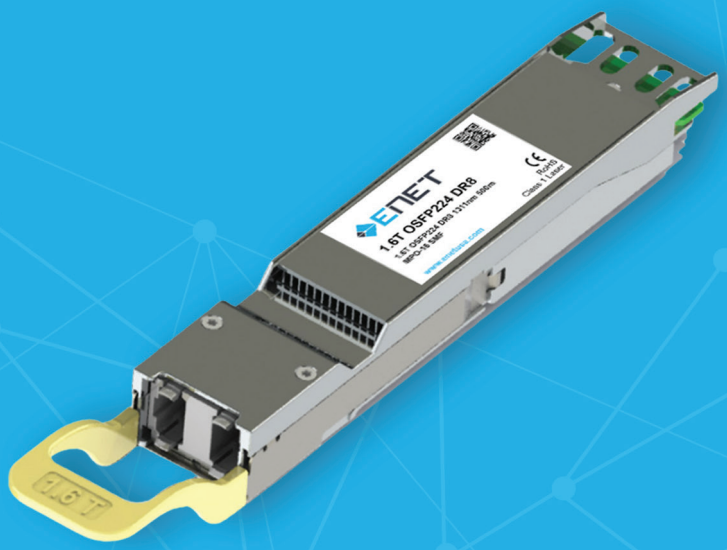
1.6T DR8 OSFP224
Transceiver

MMS400-XM-ENC

ENET 1.6TBASE-DR8 OSFP224 InfiniBand 2x800G DR4 Dual MPO-12/APC 1310nm 500m CMIS SMF IHS NVIDIA Mellanox Compatible



Legacy PN:	MMS4A00-XM-ENC - 1.6TBASE-DR8 OSFP224 InfiniBand 2x800G DR4 Dual MPO-12/APC 1310nm 500m CMIS SMF IHS NVIDIA Mellanox Compatible
NVIDIA OPN:	980-9IAH1-00XM00-ENC - 1.6TBASE-DR8 OSFP224 InfiniBand 2x800G DR4 Dual MPO-12/APC 1310nm 500m CMIS SMF IHS NVIDIA Mellanox Compatible

Introduction

This product is an 1600Gb/s Octal Small Form-factor Pluggable (OSFP) optical module with top closed fin designed for 500m optical communication applications. The module converts 8 channels of 200Gb/s (PAM4) electrical input data to 8 channels of parallel optical signals via integrated silicon photonics optical path, each capable of 200Gb/s operation for an aggregate data rate of 1600Gb/s. Reversely, on the receiver side, the module converts 8 channels of parallel optical signals of 200Gb/s each channel for an aggregate data rate of 1600Gb/s into 8 channels of 200Gb/s (PAM4) electrical output data.

An optical fiber cable with dual MPO-12 connector can be plugged into the OSFP 2x DR4 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an OSFP MSA-compliant edge type connector.

I2C interface is supported to read and control the status of this product.

Figure 1 shows the transceiver block diagram

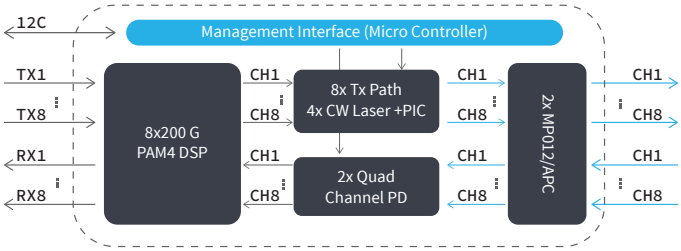


Figure 1. Transceiver Block Diagram

- OSFP form factor hot pluggable
- CMIS compliance
- 8 channels of 200G-PAM4 electrical and optical parallel lanes
- Dual Optical port of MPO-12/APC
- Top closed fin
- 500m maximum reach via single mode fiber
- 32 Watts max
- Case temperature range of 0°C to 70°C

Key Features

The transceiver complies with common management interface specification (CMIS). The supported key features listed below allow host software to read and control the transceiver status through I2C.

- Adaptive Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-cursor
- Programmable Rx output post-cursor
- Supply voltage monitoring (DDM_Voltage)
- Transceiver case temperature monitoring (DDM_ Temperature)
- Tx transmit optical power monitoring for each lane (DDM_TxPower)
- Tx bias current monitoring for each lane (DDM_ TxBias)
- Rx receive optical power monitoring for each lane (DDM_RxPower)
- Warning and alarm indication for each DDM function
- Tx & Rx LOL and LOS indication
- Tx fault indication
- Host and line side loopback capabilities
- Host and line side PRBS generator and checker capabilities
- CDB firmware upgrade capability
- Versatile diagnostics monitoring (VDM) capability (optional, additional power consumption increase)
- Other functions defined in CMIS

Pin Map and Description

The electrical interface of OSFP module consist of a 60 contacts edge connector as illustrated by the diagram in Figure 2, which defined in Clause 8.1 of OSFP MSA Specification.

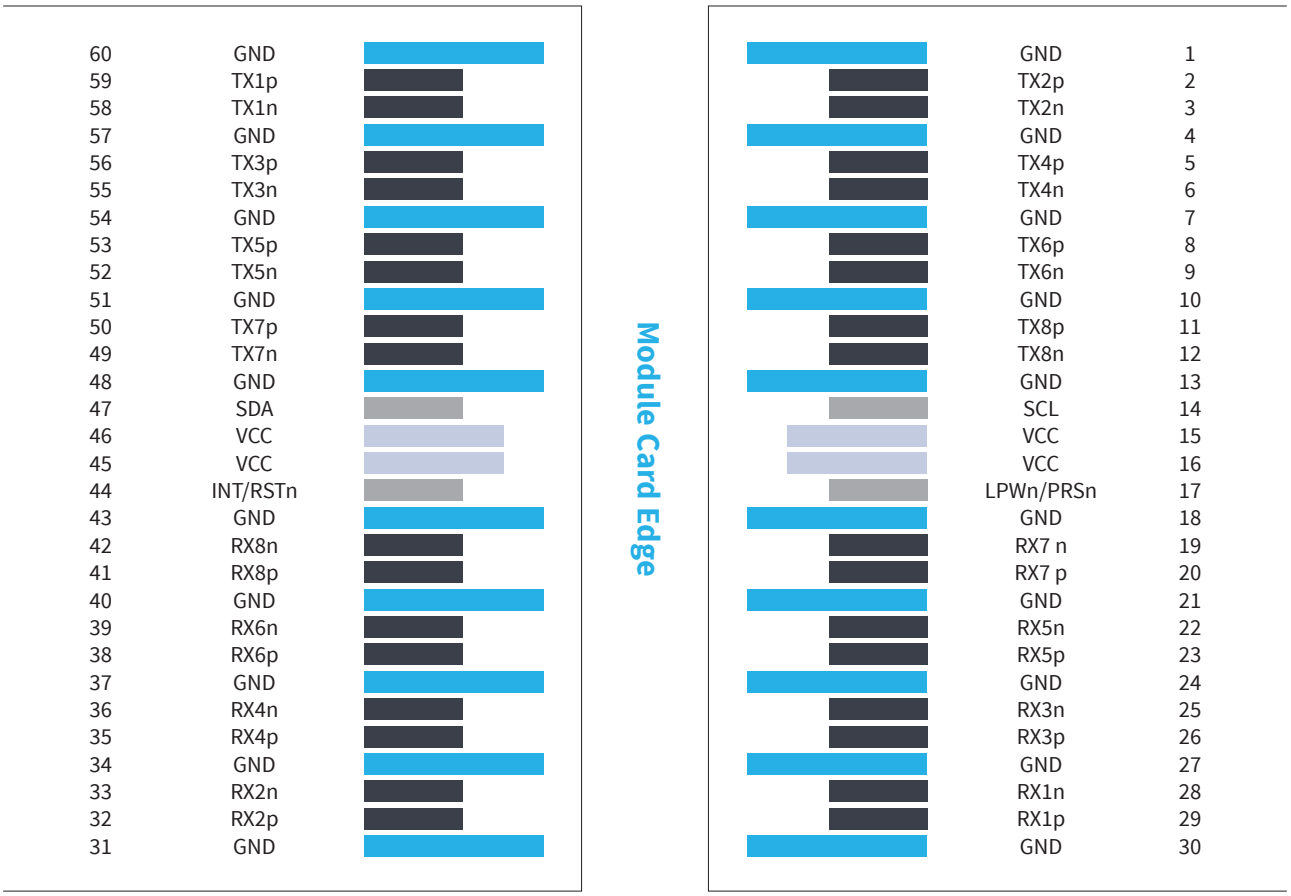


Figure 2. MSA Compliant Connector

Table 2 shows the detailed pin list

Table 2 OSFP connector pin list

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
1	GND		Ground		1
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3
4	GND		Ground		1
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3
7	GND		Ground		1
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3
10	GND		Ground		1
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3
13	GND		Ground		1
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3
15	VCC	+3.3V Power		Power from Host	2
16	VCC	+3.3V Power		Power from Host	2
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3
18	GND		Ground		1
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3
21	GND		Ground		1
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3
24	GND		Ground		1
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3
27	GND		Ground		1
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3
30	GND		Ground		1
31	GND		Ground		1
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3
34	GND		Ground		1
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3
37	GND		Ground		1
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3
40	GND		Ground		1

Pin#	Symbol	Description	Logic	Direction	Plug Sequence
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3
43	GND		Ground		1
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3
45	VCC	+3.3V Power		Power from Host	2
46	VCC	+3.3V Power		Power from Host	2
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3
48	GND		Ground		1
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
51	GND		Ground		1
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
54	GND		Ground		1
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
57	GND		Ground		1
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3
60	GND		Ground		1

Table 3 shows the detailed control pins

Table 3. OSFP Control pins

Name	Direction	Description
SCL	BiDir	2-wire serial clock signal. Requires pull-up resistor to 3.3V on host
SDA	BiDir	2-wire serial data signal. Requires pull-up resistor to 3.3V on host.
LPWn/ PRSn	Input/ Output	Dual Function Signal • Low Power mode is an active-low input signal • Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal Voltage zones is shown as figure3.
INT/ RSTn	Input/ Output	Dual Funtion Signal . Reset is an active-low input signal . Interrupt is an active-high output signal Voltage zones is shown as figure 3.

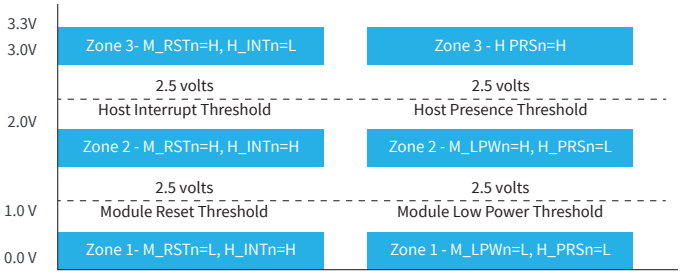


Figure 3. Voltage Zones

Figure 4 shows the recommended power supply filter design

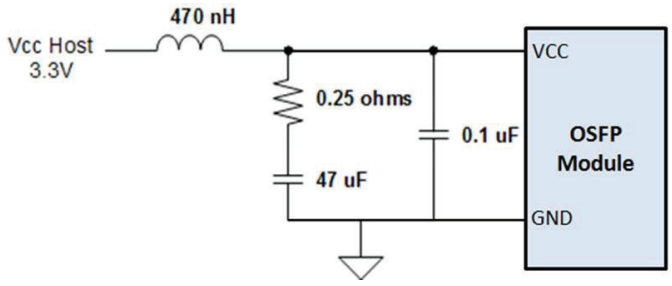


Figure 4. Recommended Power Supply Filter

Optical Port Description

The optical interface port is dual MPO-12 APC receptacle. The transmit and receive optical lanes shall occupy the positions depicted in Figure 5 when looking into the MDI receptacle with the connector keyway feature on top.

Aligned keys are used to ensure alignment between the modules and the patch cords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top. Note: Two alignment pins are present in each receptacle.

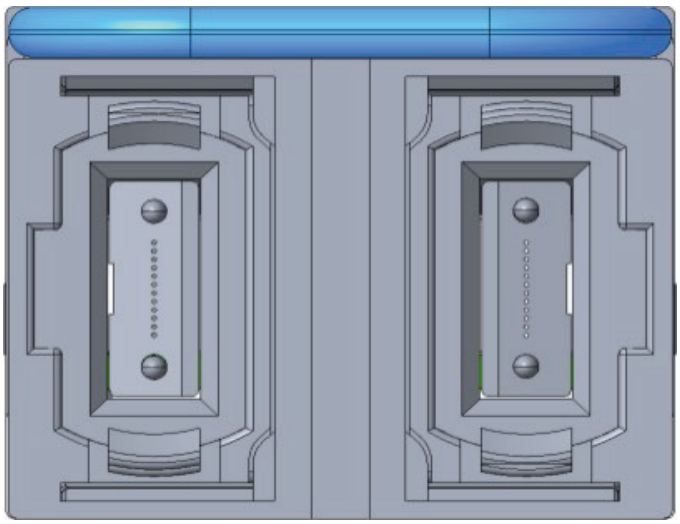


Figure 5. Optical Media Dependent Interface port assignments

Specifications

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	T_S	-40	85	degC	
Operating Case Temperature	T_{OP}	0	70	degC	PAM4
Power Supply Voltage	V_{CC}	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	T_{OP}	0		70	degC	
Power Supply Voltage	V_{CC}	3.135	3.3	3.465	V	
Data Rate, each Lane			106.25		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$1x10^{-6}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance	D			500	m	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				32	W	
Module Input (each Lane)						
Differential pk-pk input Voltage tolerance	TP1	750	-	-	mV	
Differential termination mismatch	TP1	-	-	10	%	
Single-ended voltage tolerance range	TP1	-0.4	-	3.3	V	
DC common mode Voltage	TP1	-350		2850	mV	
Module Output (each Lane)						
Peak-peak AC common-mode voltage	TP4	-	-	32	mV	
Common Mode Voltage	TP4	-350			mV	
Pk-Pk AC Common Mode Voltage Low Frequency	TP4			80	mV	
Differential output Voltage (Long mode)	TP4	-	-	845	mV	
Differential output Voltage (Short mode)	TP4	-	-	600	mV	
Eye height, differential	TP4	15	-	-	mV	
Differential Termination Mismatch	TP4	-	-	10	%	

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Notes
Center Wavelength	λc	1304.5	1311	1317.5	nm	
Transmitter						
Data Rate, each Lane			106.25 ± 100 ppm		GBd	
Modulation Format			PAM4			
Side Mode Suppression Ratio	SMSR	30			dB	
Average Launch Power, each lane	AOPL	-3.3		4	dBm	1,2
Outer Optical Modulation Amplitude (OMAouter), each lane For max(TECQ,TDCEQ) <0.9dB For 0.9dB ≤ max(TECQ,TDECQ) ≤ 3.4dB	TOMA	-0.3 -1.2+ max TECQ, TDECQ)		4.2	dBm	
Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each lane	TDECQ			3.4	dB	
TECQ	TECQ			3.4	dB	
|TDECQ- TECQ|				2.5	dB	
Transmitter overshoot/undershoot				22	%	
Average Launch Power of OFF Transmitter, each lane	TOFF			-15	dBm	
Extinction Ratio, each lane	ER	3.5			dB	
Transmitter transition time	T_t			8	ps	
RIN21.4OMA	RIN			-139	dB/Hz	
Optical Return Loss Tolerance	ORL			21.4	dB	
Transmitter Reflectance	TR			-26	dB	3

Receiver					
Data Rate, each Lane		106.25 ± 100 ppm		GBd	
Modulation Format		PAM4			
Damage Threshold, average optical power, each lane	AOPD	5		dBm	4
Average Receive Power, each lane	AOPR	-6.3	4	dBm	5
Receive Power (OMAouter), each lane	OMA-R		4.2	dBm	
Receiver Reflectance	RR		-26	dB	
Receiver Sensitivity (OMAouter), each lane	SOMA		Max (-3.4, -4.3+TECQ)	dBm	6
Stressed Receiver Sensitivity (OMAouter), each lane	SRS		-0.9	dBm	6
Conditions of stressed receiver sensitivity test (Note 7)					
Stressed eye closure for PAM4 (SECQ)		3.4		dB	
OMAouter of each aggressor lane		2.9		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength.
2. An average launch power of -3.3dBm corresponds to an OMA of -0.3 dBm with an infinite extinction ratio.
3. Transmitter reflectance is defined looking into the transmitter.
4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level. The receiver does not have to operate correctly at this input power.
5. Average receiver power, each lane (min) is not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
6. Measure with conformance test signal at TP3 for the block error ratio specified in 180.2 of IEEE 802.3dj.
7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

Digital Diagnostic Specifications

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Mechanical Drawing

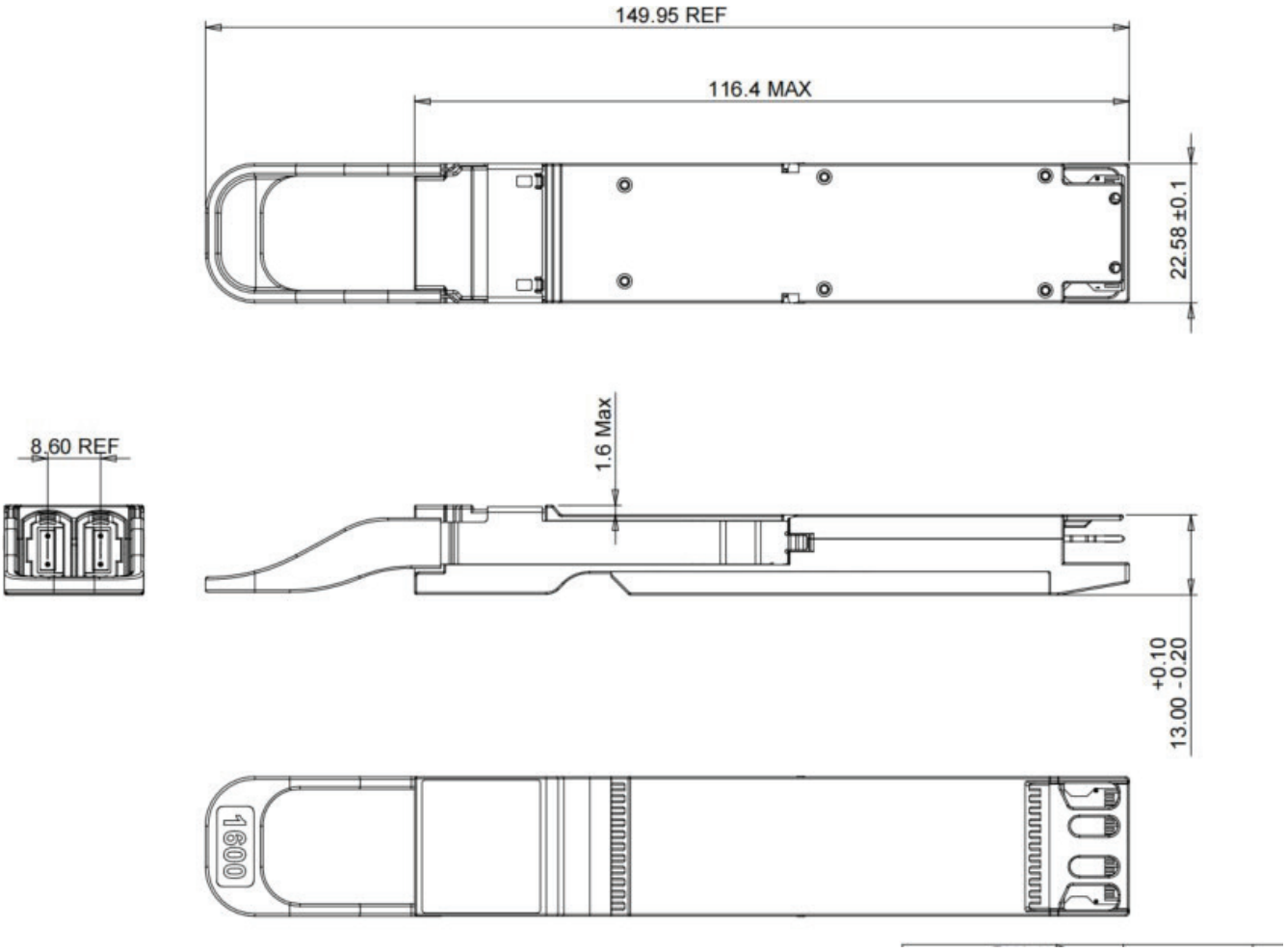


Figure 7. Mechanical Outline(IHS)

ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser safety

This is a Class I Laser Product, or Class 1 Laser Product according to IEC/EN 60825-1:2014.

This product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.