JL310A-80K-ENC

100GBASE-ZR4 QSFP28 1295/1300/1304/1309nm 80km DOM SMF Duplex LC Connector HPe/Aruba Compatible

Product Features

- Supports 103Gbps
- Single 3.3V power supply
- Power dissipation : <5W
- Up to 80km over SMF
- Commercial case temperature range of 0°C to 70°C
- Four 25Gbps EML LAN-WDM lasers on transmitter side
- SOA&PD on the receiver side
- 4x25Gbps / electrical interface
- Duplex LC receptacles
- I^2C interface with integrated Digital Diagnostic Monitoring
- Safety certification: TUV/UL/FDA
- RoHS compliant

Applications

- 100G 80km applications with FEC on host side
- 100G Datacom & Telecom connections

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit
Storage temperature	Ts	-40	+85	°C
Supply voltage	Vcc	-0.5	3.6	V
Operating relative humidity	RH	5	85	%

*Exceeding any one of these values may destroy the device immediately.

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating case temperature	T_c	0		70	°C
Power supply voltage	Vcc	3.135	3.3	3.465	V
Power dissipation	P_D			5.5	W

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Performance Specifications – Electrical

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Differential data input swing per lane				900	mv_{p-p}
Input Impedance (Differential)	Zin			10	%
Stressed input parameters					
Eye width		0.46			UI
Applied pk-pk sinusoidal jitter		IEEE 802.3bm Table 88-13			
Eye height		95			mV
DC common mode voltage		-350		2850	mV
Receiver					
Differential output amplitude		200		900	mv_{p-p}
Output Impedance (Differential)	Zout			10	%
Eye width		0.57			UI
Eye height differential		228			mV
Vertical eye closure				5.5	dB

Optical Characteristics

100GBASE Operation

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Signaling Speed per Lane	BR_{AVE}		25.78		Gbps
Data rate variation		-100		+100	ppm
Lane_0 center wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 center wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 center wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 center wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Spectral width (-20dB)	$\Delta\lambda$			1	nm
Total average output power	Po			13	dBm
Average launch power per lane*(Note4)	Peach	3		7	dBm
Optical modulation amplitude per lane	POMA	3.7		7.8	dBm

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Average launch power of OFF transmitter per lane	Poff			-30	dBm
Side-mode suppression ratio	SMSR	30			dB
Transmitter dispersion penalty , each lane*(Note6)	TDP			1	dB
Difference in launch power between any two lanes				3.6	dB
Optical Return loss tolerance				20	dB
Transmitter reflectance				-26	
Extinction ratio	ER	6	8		dB
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}*(Note8)		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}			
Receiver					
Signaling speed per lane	BR_{AVE}		25.78		Gbps
Data rate variation		-100		+100	ppm
Lane_0 center wavelength	λ_{C0}	1294.53	1295.56	1296.59	nm
Lane_1 center wavelength	λ_{C1}	1299.02	1300.05	1301.09	nm
Lane_2 center wavelength	λ_{C2}	1303.54	1304.58	1305.63	nm
Lane_3 center wavelength	λ_{C3}	1308.09	1309.14	1310.19	nm
Average receive power per lane	Rx_pow	-31		4.5	dBm
Damage threshold per lane(min) *(Note5)	Pdamage			5.5	dBm
Receiver overload per Lane	Psat	4.5			dBm
Receive sensitivity average per lane*(Note6)	Rx_sens			-29	dBm
Stressed Sensitivity per lane*(Note6)	SRS			-25.1	dBm
Receiver reflectance	ORL			-26	dB
LOS Assert	LOSA	-42			dBm
LOS De-Assert	LOSD			-31.5	dBm
LOS hysteresis		0.5			dB

Note4. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.

Note5. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.

Note6. Measured with conformance test signal for BER = 5E-5@25.78Gbps $PRBS^{31}$-1.

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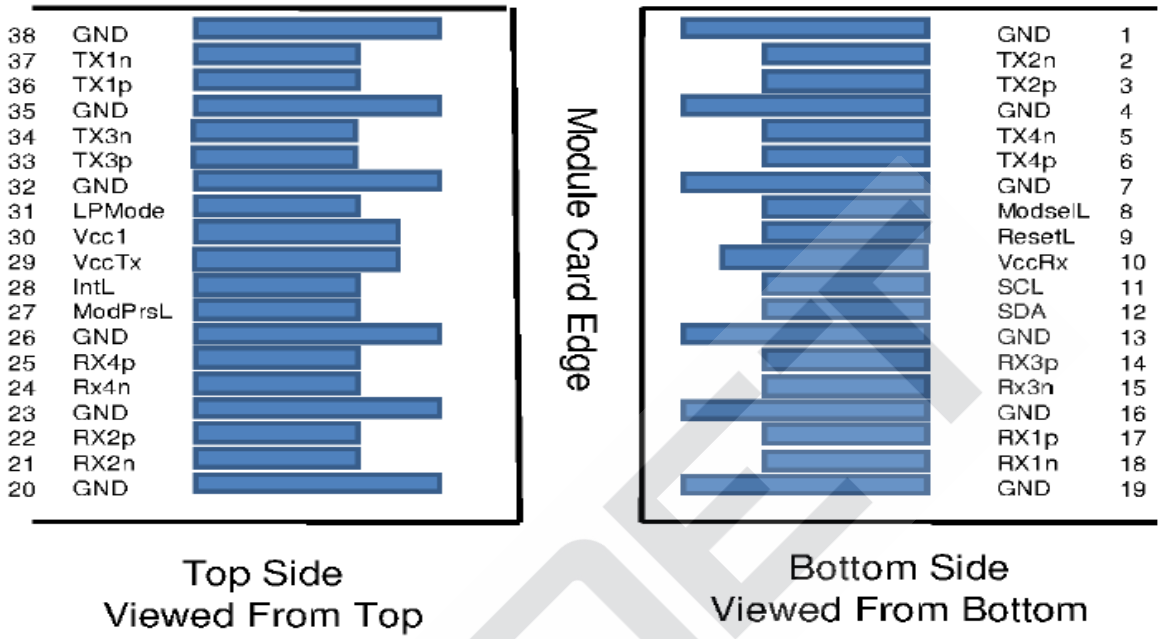
QSFP28 Transceiver Electrical Pad Layout



Pin Arrangement and Definition

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		VccRx	+3.3V Power Supply Receiver	2	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1

17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		VccTx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

1: GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the QSFP28 module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

2: Vcc Rx, Vcc1 and Vcc Tx are the receiver and transmitter power supplies and shall be applied concurrently. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the QSFP28 Module in any combination. The connector pins are each rated for a maximum current of 1000mA.

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Mechanical Specifications