

OSFP-800G-2DR4-ENC



800GBASE-DR8 OSFP112 1310nm 500m DOM SMF Dual DR4
MPO/MTP-12 APC Commercial Temp Arista Compatible

Introduction

This product is an 800Gb/s Octal Small Form-factor Pluggable (OSFP) optical module with top closed fin designed for 500m optical communication applications. The module converts 8 channels of 100Gb/s (PAM4) electrical input data to 8 channels of parallel optical signals via integrated silicon photonics optical path, each capable of 100Gb/s operation for an aggregate data rate of 800Gb/s. Reversely, on the receiver side, the module converts 8 channels of parallel optical signals of 100Gb/s each channel for an aggregate data rate of 800Gb/s into 8 channels of 100Gb/s (PAM4) electrical output data.

An optical fiber cable with dual MPO-12 connector can be plugged into the OSFP112 DR8 module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through an OSFP MSA-compliant edge type connector.

I2C interface is supported to read and control the status of this product.

Figure 1 shows the transceiver block diagram

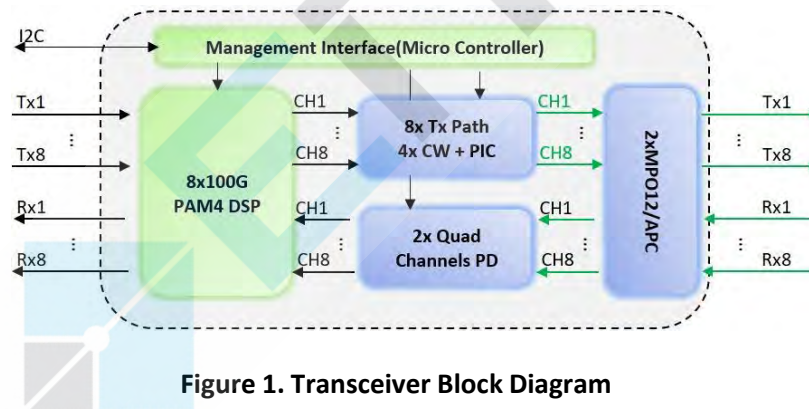


Figure 1. Transceiver Block Diagram

- OSFP form factor hot pluggable
- CMIS compliance
- 8 channels of 100G-PAM4 electrical and optical parallel lanes
- Dual Optical port of MPO-12/APC
- Top closed fin
- 500m maximum reach via single mode fiber
- 15 Watts max
- Case temperature range of 0°C to 70°C



OSFP-800G-2DR4-ENC



Key Features

The transceiver complies with common management interface specification (CMIS). The supported key features listed below allow host software to read and control the transceiver status through I2C.

- Adaptive Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-cursor
- Programmable Rx output post-cursor
- Supply voltage monitoring (DDM_Voltage)
- Transceiver case temperature monitoring (DDM_Temperature)
- Tx transmit optical power monitoring for each lane (DDM_TxPower)
- Tx bias current monitoring for each lane (DDM_TxBias)
- Rx receive optical power monitoring for each lane (DDM_RxPower)
- Warning and alarm indication for each DDM function
- Tx & Rx LOL and LOS indication
- Tx fault indication
- Host and line side loopback capabilities
- Host and line side PRBS generator and checker capabilities
- CDB firmware upgrade capability
- Versatile diagnostics monitoring (VDM) capability (optional, additional power consumption increase)
- Other functions defined in CMIS

Applications

The transceiver is designed for Ethernet, Telecom and Infiniband use cases. The application advertisements listed below allow host software to select proper application following CMIS definition

- Application case 1, 8x100G DR, 8 of 100G per channel breakout connections.
- Application case 2, 2x400G DR4, 2 of 400G per port breakout connections.
- Application case 3, 2x200G DR4, 2 of 200G per port breakout connections.
- Application case 4, 1x800G DR8, 1 of 800G per port point to point connection.
- Application case 5, 2x100G PSM4, 2 of 100G per port breakout connections.
- Applications for backward compliance, refer to detailed application list below.

Key Features

The transceiver complies with common management interface specification (CMIS). The supported key features listed below allow host software to read and control the transceiver status through I2C.

- Adaptive Tx input equalization
- Programmable Rx output amplitude
- Programmable Rx output pre-cursor
- Programmable Rx output post-cursor
- Supply voltage monitoring (DDM_Voltage)
- Transceiver case temperature monitoring (DDM_Temperature)
- Tx transmit optical power monitoring for each lane (DDM_TxPower)
- Tx bias current monitoring for each lane (DDM_TxBias)
- Rx receive optical power monitoring for each lane (DDM_RxPower)
- Warning and alarm indication for each DDM function
- Tx & Rx LOL and LOS indication
- Tx fault indication
- Host and line side loopback capabilities
- Host and line side PRBS generator and checker capabilities
- CDB firmware upgrade capability
- Versatile diagnostics monitoring (VDM) capability (optional, additional power consumption increase)
- Other functions defined in CMIS

Applications

The transceiver is designed for Ethernet, Telecom and Infiniband use cases. The application advertisements listed below allow host software to select proper application following CMIS definition

- Application case 1, 8x100G DR, 8 of 100G per channel breakout connections.
- Application case 2, 2x400G DR4, 2 of 400G per port breakout connections.
- Application case 3, 2x200G DR4, 2 of 200G per port breakout connections.
- Application case 4, 1x800G DR8, 1 of 800G per port point to point connection.
- Application case 5, 2x100G PSM4, 2 of 100G per port breakout connections.
- Applications for backward compliance, refer to detailed application list below.

Mixed applications of case 1 and case 2 are also supported.

Table 1 shows CMIS application advertisements list:

Table 1. CMIS Application advertisements

| ApSel Code | Host Electrical Interface | Module Media Interface | Host and Media Lane Count | Host Lane Assignment |
|------------|-----------------------------|------------------------|---------------------------|----------------------------|
| ApSel 1 | 50 (400GAUI-4-L C2M) | 1C (400GBASE-DR4) | 44 (4:4) | 11 (lanes 1,5) |
| ApSel 2 | 32 (IB NDR) | 1C (400GBASE-DR4) | 44 (4:4) | 11 (lanes 1,5) |
| ApSel 3 | F (200GAUI-4 C2M) | 17 (200GBASE-DR4) | 44 (4:4) | 11 (lanes 1,5) |
| ApSel 4 | 31 (IB HDR) | 17 (200GBASE-DR4) | 44 (4:4) | 11 (lanes 1,5) |
| ApSel 5 | 4C (100GAUI-1-L C2M) | 14 (100GBASE-DR) | 11 (1:1) | FF (lanes 1,2,3,4,5,6,7,8) |
| ApSel 6 | 52 (800GAUI-8-L C2M) | 0 (Undefined) | 88 (8:8) | 01 (lane 1) |
| ApSel 7 | 4F (400GAUI-4-S C2M) | 1C (400GBASE-DR4) | 44 (4:4) | 11 (lanes 1,5) |
| ApSel 8 | 4B (100GAUI-1-S C2M) | 14 (100GBASE-DR) | 11 (1:1) | FF (lanes 1,2,3,4,5,6,7,8) |
| ApSel 9 | 51 (800GAUI-8-S C2M) | 0 (Undefined) | 88 (8:8) | 01 (lane 1) |
| ApSel 10 | 42 (CAUI-4 C2M with RS FEC) | F (100G PSM4 MSA) | 44 (4:4) | 11 (lanes 1,5) |
| ApSel 11 | 30 (IB EDR) | F (100G PSM4 MSA) | 44 (4:4) | 11 (lanes 1,5) |

4. Pin Map and Description

The electrical interface of OSFP module consist of a 60 contacts edge connector as illustrated by the diagram in Figure 2, which defined in Clause 8.1 of OSFP MSA Specification.

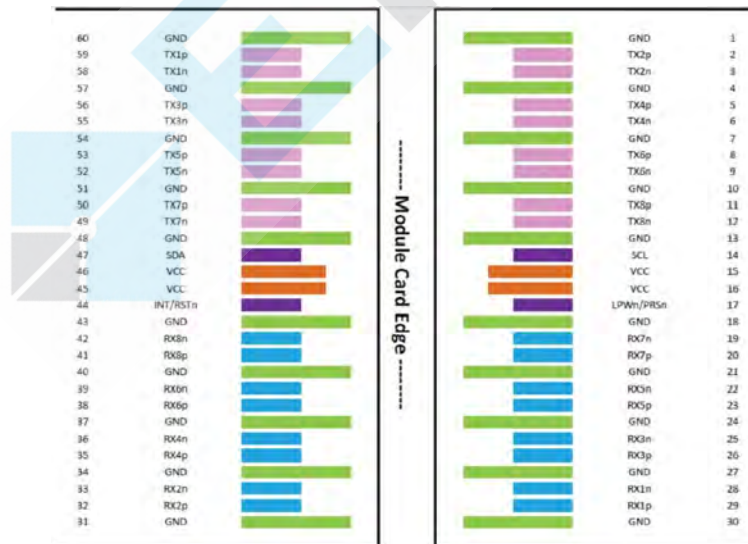


Figure 2. MSA Compliant Connector

Table 2 shows the detailed pin list

Table 2 OSFP connector pin list

| Pin# | Symbol | Description | Logic | Direction | Plug Sequence |
|------|-----------|---------------------------------|-------------|-----------------|---------------|
| 1 | GND | | Ground | | 1 |
| 2 | TX2p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 3 | TX2n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 4 | GND | | Ground | | 1 |
| 5 | TX4p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 6 | TX4n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 7 | GND | | Ground | | 1 |
| 8 | TX6p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 9 | TX6n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 10 | GND | | Ground | | 1 |
| 11 | TX8p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 12 | TX8n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 13 | GND | | Ground | | 1 |
| 14 | SCL | 2-wire Serial interface clock | LVC MOS-I/O | Bi-directional | 3 |
| 15 | VCC | +3.3V Power | | Power from Host | 2 |
| 16 | VCC | +3.3V Power | | Power from Host | 2 |
| 17 | LPWn/PRSn | Low-Power Mode / Module Present | Multi-Level | Bi-directional | 3 |
| 18 | GND | | Ground | | 1 |
| 19 | RX7n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 20 | RX7p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 21 | GND | | Ground | | 1 |
| 22 | RX5n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 23 | RX5p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 24 | GND | | Ground | | 1 |
| 25 | RX3n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 26 | RX3p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 27 | GND | | Ground | | 1 |
| 28 | RX1n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 29 | RX1p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 30 | GND | | Ground | | 1 |
| 31 | GND | | Ground | | 1 |
| 32 | RX2p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 33 | RX2n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 34 | GND | | Ground | | 1 |
| 35 | RX4p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 36 | RX4n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 37 | GND | | Ground | | 1 |
| 38 | RX6p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 39 | RX6n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 40 | GND | | Ground | | 1 |
| 41 | RX8p | Receiver Data Non-Inverted | CML-O | Output to Host | 3 |
| 42 | RX8n | Receiver Data Inverted | CML-O | Output to Host | 3 |
| 43 | GND | | Ground | | 1 |
| 44 | INT/RSTn | Module Interrupt / Module Reset | Multi-Level | Bi-directional | 3 |
| 45 | VCC | +3.3V Power | | Power from Host | 2 |

| | | | | | |
|----|------|-------------------------------|-------------|-----------------|---|
| 46 | VCC | +3.3V Power | | Power from Host | 2 |
| 47 | SDA | 2-wire Serial interface data | LVC MOS-I/O | Bi-directional | 3 |
| 48 | GND | | Ground | | 1 |
| 49 | TX7n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 50 | TX7p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 51 | GND | | Ground | | 1 |
| 52 | TX5n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 53 | TX5p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 54 | GND | | Ground | | 1 |
| 55 | TX3n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 56 | TX3p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 57 | GND | | Ground | | 1 |
| 58 | TX1n | Transmitter Data Inverted | CML-I | Input from Host | 3 |
| 59 | TX1p | Transmitter Data Non-Inverted | CML-I | Input from Host | 3 |
| 60 | GND | | Ground | | 1 |

Table 3 shows the detailed control pins

Table 3. OSFP Control pins

| Name | Direction | Description |
|-----------|--------------|--|
| SCL | BiDir | 2-wire serial clock signal. Requires pull-up resistor to 3.3V on host |
| SDA | BiDir | 2-wire serial data signal. Requires pull-up resistor to 3.3V on host. |
| LPWn/PRSn | Input/Output | Dual Function Signal . Low Power mode is an active-low input signal . Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low output logic signal Voltage zones is shown as figure3. |
| INT/RSTn | Input/Output | Dual Function Signal . Reset is an active-low input signal . Interrupt is an active-high output signal Voltage zones is shown as figure 3. |

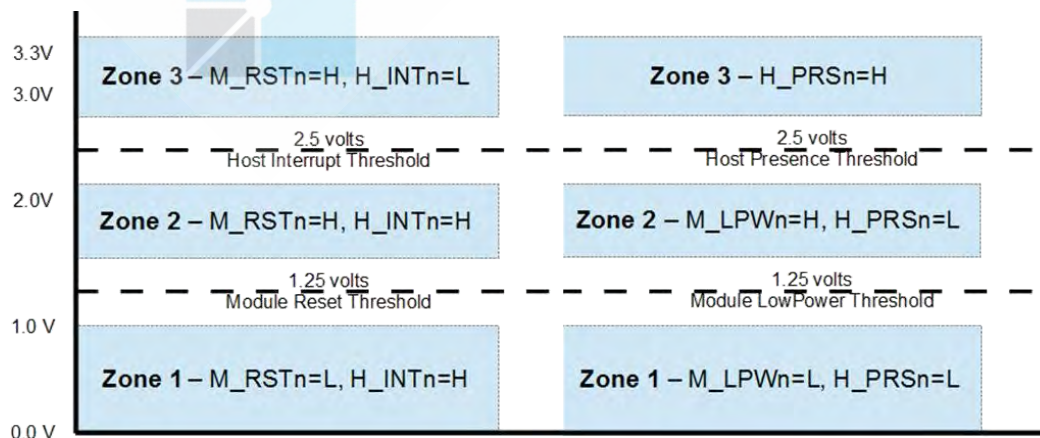


Figure 3. Voltage Zones

Figure 4 shows the recommended power supply filter design

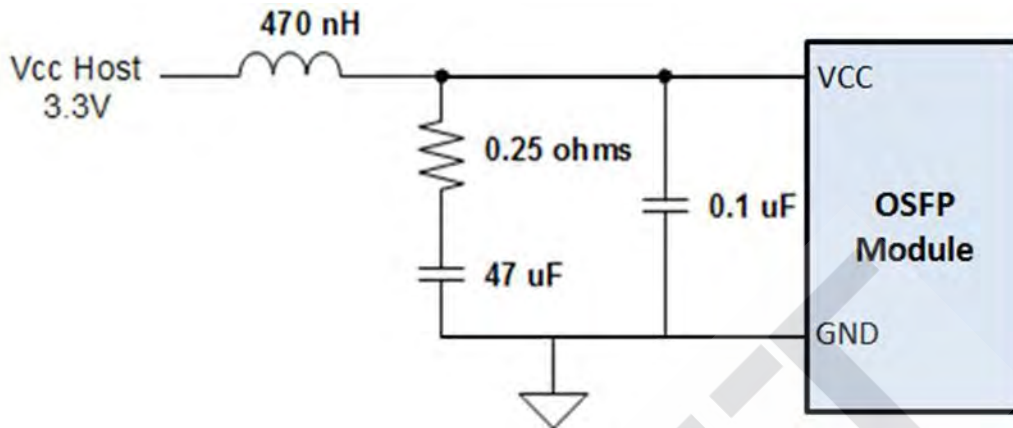


Figure 4. Recommended Power Supply Filter

Optical Port Description

The optical interface port is dual MPO-12 APC receptacle. The transmit and receive optical lanes shall occupy the positions depicted in Figure 5 when looking into the MDI receptacle with the connector keyway feature on top.

Aligned keys are used to ensure alignment between the modules and the patch cords. The optical connector is orientated such that the keying feature of the MPO receptacle is on the top. Note: Two alignment pins are present in each receptacle.

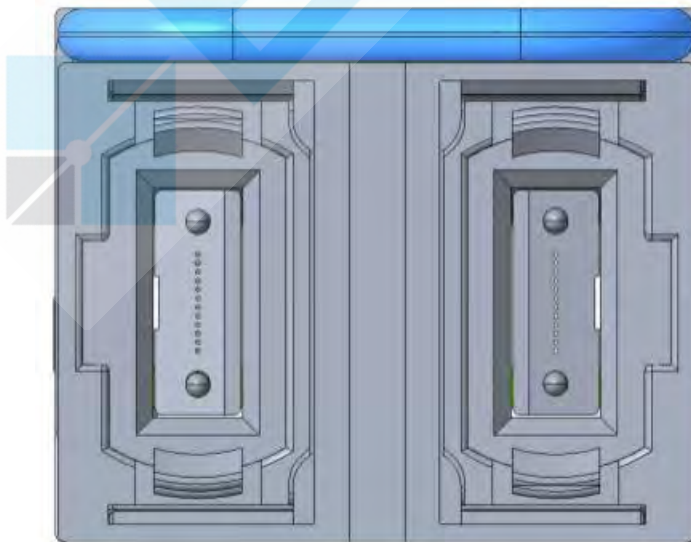


Figure 5. Optical Media Dependent Interface port assignments

Specification

Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

| Parameter | Symbol | Min | Max | Units | Notes |
|--------------------------------------|----------|------|-----|-------|-------|
| Storage Temperature | T_S | -40 | 85 | degC | |
| Operating Case Temperature | T_{OP} | 0 | 70 | degC | |
| Power Supply Voltage | V_{CC} | -0.5 | 3.6 | V | |
| Relative Humidity (non-condensation) | RH | 0 | 85 | % | |

Recommended Operating Conditions

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|----------------------------|----------|-------|---------|----------------------|-------|-------|
| Operating Case Temperature | T_{OP} | 0 | | 70 | degC | |
| Power Supply Voltage | V_{CC} | 3.135 | 3.3 | 3.465 | V | |
| Data Rate, each Lane | | | 53.125 | | GBd | PAM4 |
| Data Rate Accuracy | | -100 | | 100 | ppm | |
| Pre-FEC Bit Error Ratio | | | | 2.4×10^{-4} | | |
| Post-FEC Bit Error Ratio | | | | 1×10^{-15} | | 1 |
| Link Distance | D | 2 | | 500 | m | 2 |

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

| Parameter | Test Point | Min | Typical | Max | Units | Notes |
|--|------------|----------------------|---------|------|-------|-------|
| Power Consumption | | | | 15 | W | |
| Module Input (each Lane) | | | | | | |
| Signaling Rate, each Lane | TP1 | 53.125 ± 100 ppm | | | GBd | |
| DC Common-mode input Voltage | TP1 | -0.35 | | 2.85 | V | |
| Single-ended input Voltage | TP1a | -0.4 | | 3.3 | V | |
| AC Common-mode RMS input Voltage Low-frequency, $V_{CM_{LF}}$ Full-Band, $V_{CM_{LF}}$ | TP1a | 32 80 | | | mV | |

| | | | | | | |
|--|------|-----------------------------|--|------------|-----|--|
| Module stressed input test | | IEEE 802.3ck 120G3.4.3 | | | | |
| Differential Peak-to-Peak input Voltage tolerance | TP1a | 750 | | | mV | |
| Common to Different Mode input Return Loss | TP1 | IEEE802.3ck Equation 120G-2 | | | | |
| Effective input Return Loss | TP1 | 8.5 | | | dB | |
| Differential input Termination Mismatch | TP1 | | | 10 | % | |
| Module Output (each Lane) | | | | | | |
| Signaling Rate, each lane | TP4 | 53.125 ± 100 ppm | | | GBd | |
| Differential Peak-to-Peak Output Voltage Short mode Long mode | TP4 | | | 600 845 | mV | |
| AC Common Mode Output Voltage, RMS Low-frequency, $V_{CM_{LF}}$ Full-Band, $V_{CM_{LF}}$ | TP4 | | | 32 80 | mV | |
| Differential Termination Mismatch | TP4 | | | 10 | % | |
| Eye height | TP4 | 15 | | | mV | |
| Vertical eye closure, VEC | TP4 | | | 12 | dB | |
| Common-mode to Differential mode output Return Loss | TP4 | IEEE802.3ck Equation 120G-1 | | | dB | |
| Effective output Return Loss | TP4 | 8.5 | | | dB | |
| Output Transition time (20% to 80%) | TP4 | 8.5 | | | ps | |
| DC Common-mode output Voltage | TP4 | -350 | | 2850 | mV | |
| Differential termination mismatch | TP4 | | | 10 | % | |

Optical Characteristics

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|-----------------|----------------------|---------|--------|-------|-------|
| Center Wavelength | λ_c | 1304.5 | 1311 | 1317.5 | nm | |
| Transmitter | | | | | | |
| Data Rate, each Lane | | 53.125 \pm 100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| Side-mode Suppression Ratio | SMSR | 30 | | | dB | |
| Average Launch Power, each Lane | P_{AVG} | -2.9 | | 4 | dBm | 1 |
| Outer Optical Modulation Amplitude (OMA _{outer}), each Lane | P_{OMA} | -0.8 | | 4.2 | dBm | 2 |
| Launch power in OMA _{outer} minus TDECQ For ER \geq 5dB For ER < 5dB | | -2.2 -1.9 | | | dB | |
| Transmitter and Dispersion Eye Closure for PAM4 (TDECQ), each Lane | TDECQ | | | 3.4 | dB | |
| Extinction Ratio | ER | 3.5 | | | dB | |
| RIN _{15.5OMA} | RIN | | | -136 | dB/Hz | |
| Optical Return Loss Tolerance | TOL | | | 15.5 | dB | |
| Transmitter Reflectance | R_T | | | -26 | dB | |
| Transmitter Transition Time | | | | 17 | ps | |
| Average Launch Power of OFF Transmitter, each Lane | P_{off} | | | -15 | dBm | |
| Receiver | | | | | | |
| Data Rate, each Lane | | 53.125 \pm 100 ppm | | | GBd | |
| Modulation Format | | PAM4 | | | | |
| Damage Threshold, each Lane | TH _d | 5 | | | dBm | 3 |
| Average Receive Power, each Lane | | -5.9 | | 4 | dBm | 4 |

| | | | | | | |
|--|-------|-----|-----|--------------|-----|---|
| Receive Power (OMA_{outer}), each Lane | | | | 4.2 | dBm | |
| Receiver Sensitivity (OMA_{outer}), each Lane | SEN | | | Equation (1) | dBm | 5 |
| Stressed Receiver Sensitivity (OMA_{outer}), each Lane | SRS | | | -1.9 | dBm | 6 |
| Receiver Reflectance | R_R | | | -26 | dB | |
| LOS Assert | LOSA | -15 | | -9.9 | dBm | |
| LOS De-assert | LOSD | | | -6.9 | dBm | |
| LOS Hysteresis | LOSH | 0.5 | | | dB | |
| Conditions of Stress Receiver Sensitivity Test (Note 7) | | | | | | |
| Stressed Eye Closure for PAM4 (SECQ), Lane under Test | | | 3.4 | | dB | |
| SECQ- $10\log_{10}(C_{eq})$ | | | | 3.4 | dB | |

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance.
2. The values for $OMA_{outer}(\min)$ vary with TDECQ. Figure 6 illustrates this along with the values for $OMA_{outer}(\max)$.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.
4. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
5. Receiver sensitivity (OMA_{outer}) is informative and is defined for a transmitter with a value of TECQ up to 3.4 dB. Receiver sensitivity should meet Equation (1), which is illustrated in Figure 6.

$$S = \max(-3.9, TC - 5.3) B \quad (1)$$

Where:

RS is the receiver sensitivity, and

TECQ is the TECQ of the transmitter used to measure the receiver sensitivity.

6. Measured with conformance test signal at TP3 for the BER equal to 2.4×10^{-4} .

7. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

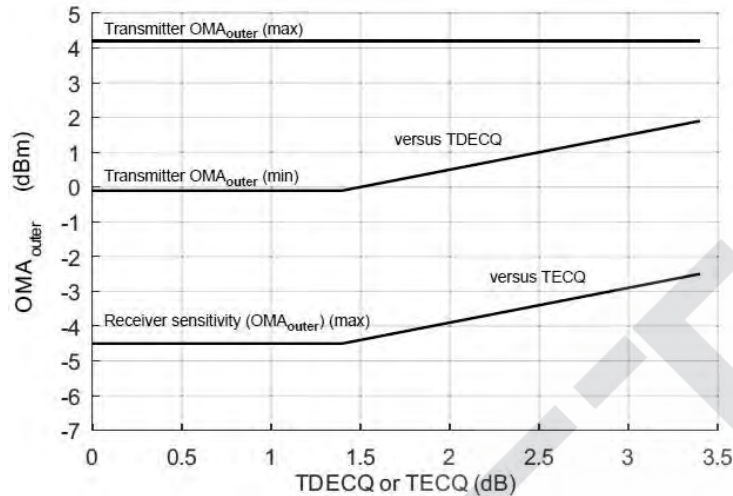


Figure 6. Illustration of Transmitter OMA_{outer} and Receiver Sensitivity Mask for 800G-DR8+

Digital Diagnostic Specifications

The following digital diagnostic characteristics are defined over the normal operating conditions unless otherwise specified.

| Parameter | Symbol | Min | Max | Units | Notes |
|---|--------------|------|-----|-------|----------------------------------|
| Temperature monitor absolute error | DMI_Temp | -3 | 3 | degC | Over operating temperature range |
| Supply voltage monitor absolute error | DMI_VCC | -0.1 | 0.1 | V | Over full operating range |
| Channel RX power monitor absolute error | DMI_RX_Ch | -2 | 2 | dB | 1 |
| Channel Bias current monitor | DMI_Ibias_Ch | -10% | 10% | mA | |
| Channel TX power monitor absolute error | DMI_TX_Ch | -2 | 2 | dB | 1 |

Notes:

- Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Mechanical Drawing

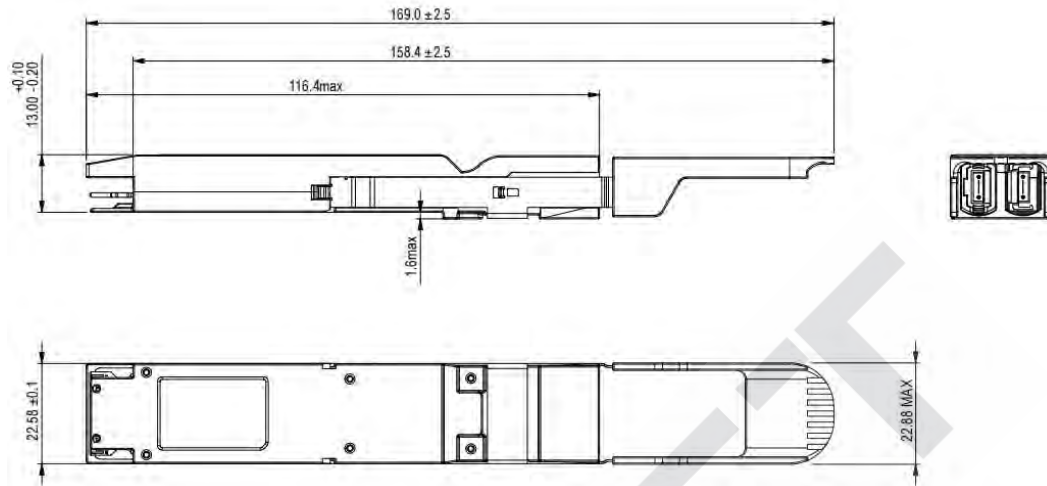


Figure 7. Mechanical Outline

ESD

This transceiver is specified as ESD threshold 1kV for high speed data pins and 2kV for all other electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

Laser safety

This is a Class I Laser Product, or Class 1 Laser Product according to IEC/EN 60825-1:2014.

This product complies with 21 CFR 1040.10 and 1040.11 except for conformance with IEC 60825-1 Ed. 3., as described in Laser Notice No. 56, dated May 8, 2019.

Caution: Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.